AN OVERLOAD PROTECTED LOW-NOISE X-BAND FET AMPLIFIER

E.C. Niehenke
T.E. Steigerwald

Westinghouse Defense and Electronics Center
Systems Development Divisions
P.O. Box 746
Baltimore, Maryland 21203

ABSTRACT

Design and performance of a 40 dB gain X-band low-noise FET amplifier with integral overload protection is presented. Noise figures as low as 2 dB have been achieved using packaged transistors, including a multidiode overload protector that protects the FET's for input pulse powers to 1 kW. Performance is achieved by the use of new embedment circuits for super-low-noise packaged FET and pin diodes in aluminum-clad soft microstrip.

INTRODUCTION

Low noise FET amplifiers are key elements in modern microwave receiver systems. Protecting the FET's from degradation due to extraneous high power input signals requires a fast-acting overload protector with low insertion loss and high power handling capability. In the past, input solid-state receiver protectors were generally implemented on separate alumina substrates using chip devices or in separate hermetic modules resulting in non-optimum overall noise figure.[1] In addition, external noise diode calibration circuits have usually added to further degradation in overall noise figure.

This paper reports techniques developed to integrate packaged pin diodes and noise diodes with the latest low-noise packaged 0.3 micron recessed gate FET's in a single aluminum-clad soft microstrip assembly, producing super-low noise with excellent protection from high input powers. This amplifier in its hermetic enclosure offers ease of manufacture and high reliability.

DESCRIPTION

Low-Noise Amplifier Module

Figure 1 illustrates the 2 dB noise figure, 40 dB gain, X-band module consisting of a waveguide input isolator with 0.1 dB loss mounted directly to the hermetic soft microstrip amplifier module. This amplifier module contains a two-stage limiter, noise diode circuit, four-stage FET amplifier, gated attenuator, and output microstrip isolator. These five circuits are integrated on a one-piece low-loss microstrip assembly that consists of 0.015 inch thick 5880 Duroid laminated to a 0.125 inch thick aluminum ground plane with a 1 ounce rolled copper conductor pattern. The input microstrip circuit contains a fast-acting two-stage passive detector driven limiter as well as a noise diode injection circuit. The latter circuit consists of a shunt-mounted silicon noise diode cascaded by a microstrip isolator to protect the diode from overload leakage signals. This noise circuit is capacitively coupled (−23 dB) to the main line, producing 11 dB excess noise ratio (ENR). A 115 dB isolation mode is incorporated into the assembly to attenuate any extraneous input signals that could be present during system calibration. This high isolation is achieved by removing the FET operating voltages and activating the input limiter and output attenuator stages.

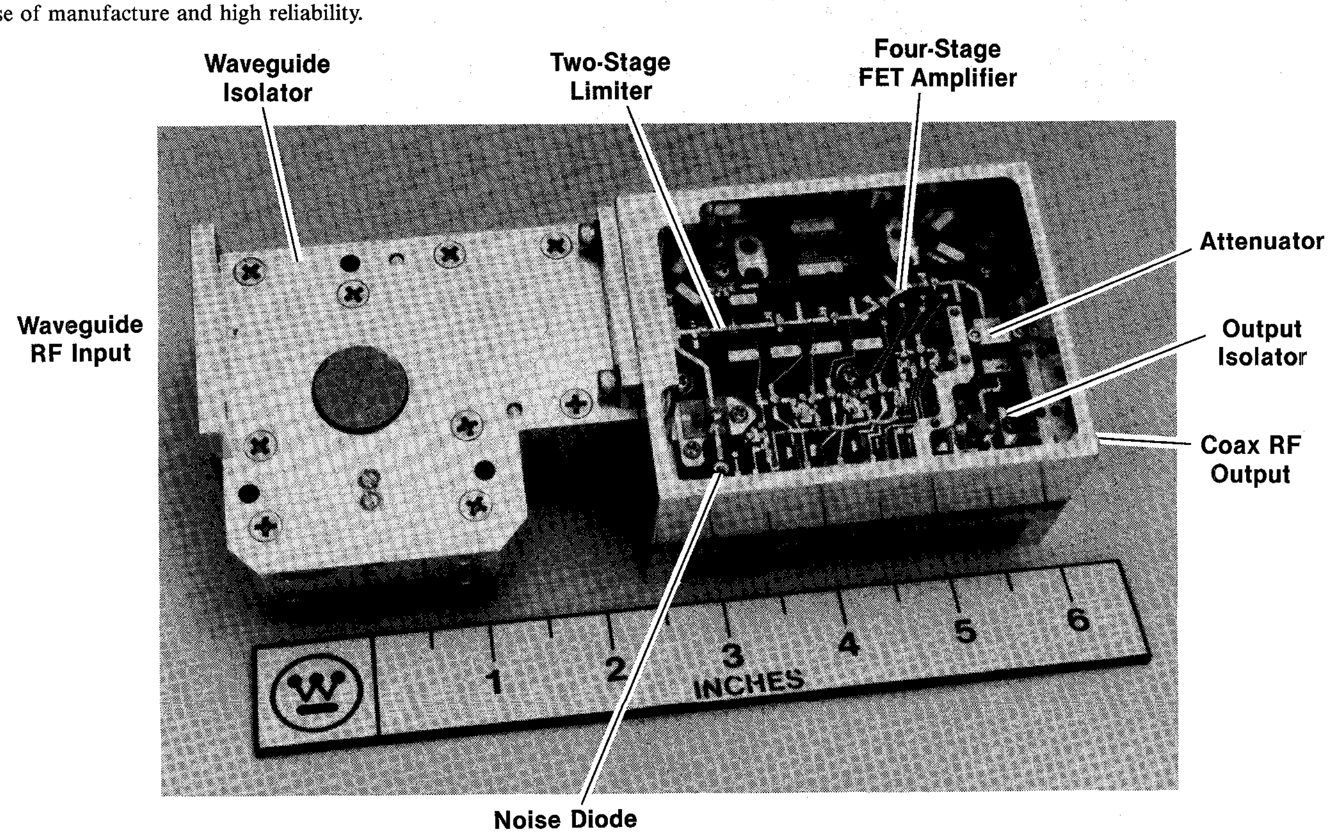

Figure 1. X-Band Low-Noise Amplifier

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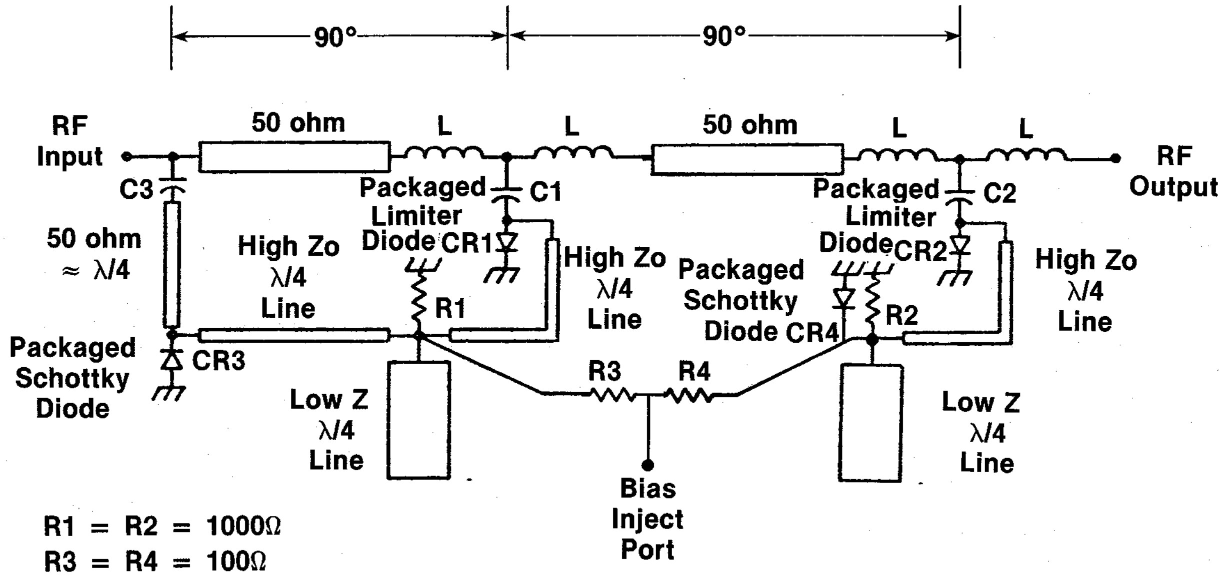
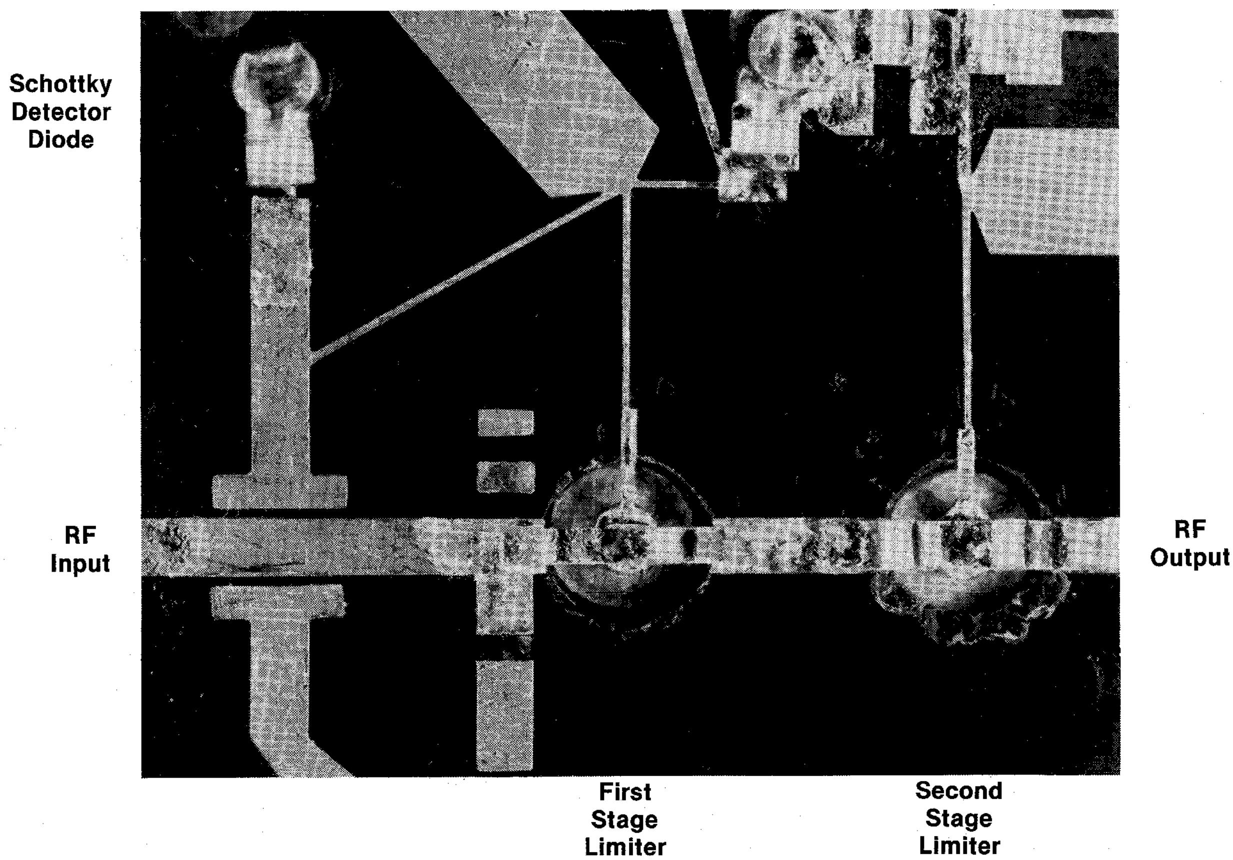
Limiter Circuit

Figure 2a illustrates the schematic of the two-stage limiter while figure 2b depicts the layout. The input limiter diode CR1 is a 12-micron basewidth device with a low thermal resistance of 22°C/watt used to reliably limit 1 kW input RF pulses. The passive limiting action of this diode is speeded up with the high breakdown voltage (70 V) silicon Schottky detector diode CR3, which detects the presence of RF through the capacitive coupler C3 and rapidly applies self-rectified current to the input limiter diode. This Schottky injection circuit places the input limiter diode in a high isolation state over a wide input power range. Pulses with high average power content are effectively and passively limited with low junction temperature rise of the limiter diode. The limiter can reliably handle CW signals to 30 watts.

The second-stage limiter diode (CR2) is a 2-micron basewidth limiter diode used to clean up the leakage signal from the first-stage limiter. The Schottky diode in this stage merely provides a dc return path for the current generated by CR2 while self-limiting. A bias injection port is provided to drive the diodes with forward current during the high isolation test mode.



a. Schematic



b. Layout

Figure 2. Two-Stage Limiter

The key embedment details used to obtain low loss, high isolation, and low thermal resistance of the limiter are shown in figure 3. The limiter diodes are encased in a low parasitic package (package capacitance of 0.12 pF, package inductance of 0.1 nH, Alpha Industries 315-001), which is screwed into the aluminum ground plane. The metal parts of the package are of gold-plated copper for low thermal resistance. The inductance of the package is resonated for maximum isolation characteristics by a parallel plate capacitor of about 3 pF soldered to the top of the diode. A narrow strap connected between the diode and bias line provides the dc return path. Finally, a contact strap of precise width (inductance) is soldered from the RF microstrip lines to the capacitor top, forming a broadband matched low-pass filter in the low-loss state.

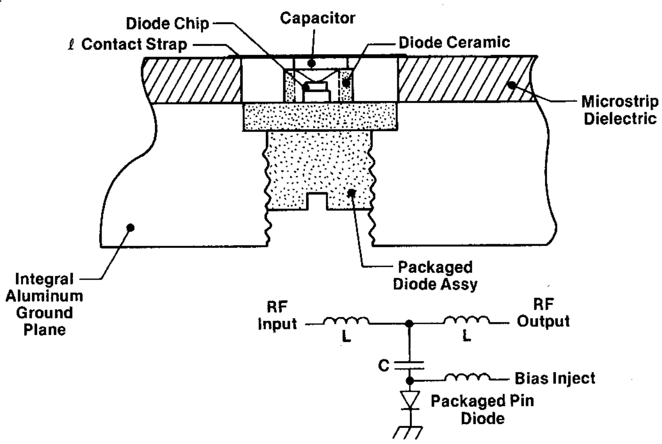


Figure 3. Packaged Pin Diode Embedment Details

Figure 4 illustrates the low insertion loss (0.43 dB) and high isolation characteristics (60 dB with 10 mA per diode) of the two-stage limiter. Figure 5 shows the flat and peak spike leakage for this limiter when subjected to a 1 μs wide pulse with a 5 ns rise time. The Schottky diode starts activating the first limiter diode at 25 dBm input

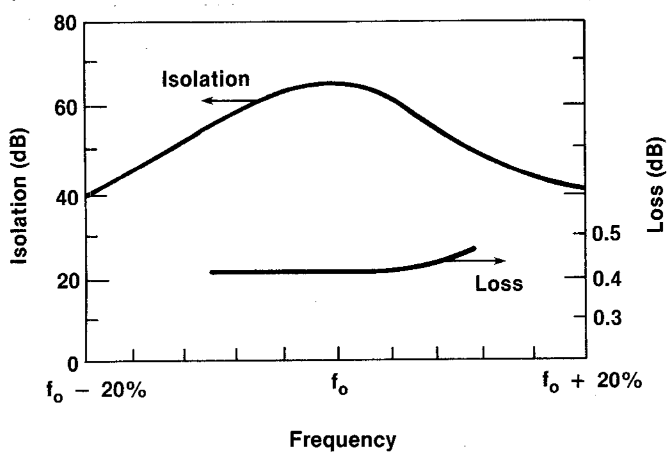


Figure 4. Isolation and Attenuation vs Frequency for Driven Two-Stage X-Band Limiter

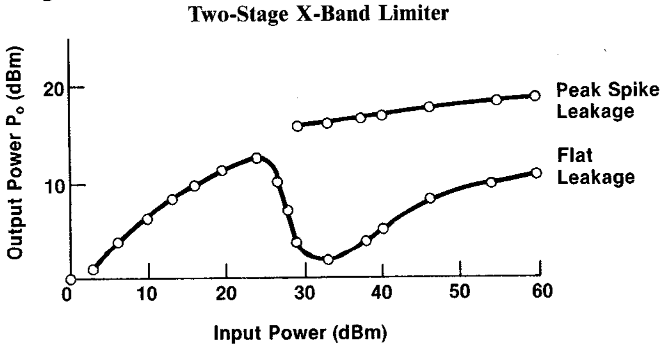


Figure 5. Isolation Characteristics for X-Band Two-Stage Detector-Driven Limiter

power, causing a rapid increase in attenuation. The peak flat and spike leakage powers are 20 and 90 mW respectively for input powers to 1 kW. This limiter was also subjected to 3 ns wide pulses for powers up to 500 watts with a maximum output peak spike power of 90 mW. The leakage powers are well below measured burnout levels of FET's (1.5-6 watts), resulting in high reliability operation.[2] The recovery time for the loss to reach the small-signal loss plus 0.5 dB varied between 60 ns at 0.25 watt input to 1200 ns at 530 watts input.

Amplifier Circuit

Super-low-noise amplification is achieved through the use of an input 0.3-micron recessed-gate NE 67383 FET coupled with a low-loss input matching network. The intrinsic noise figure of the transistor biased for low noise is 1.1 dB over a 10 percent operating range at X-band. A short length of high-impedance line in series with a parallel plate capacitor (dc block) to ground directly in front of the FET provides optimum noise figure. The capacitor is chosen to be series-resonant at the center operating frequency, f_o. This circuit gives excellent performance over a 10 percent bandwidth. The remaining three FET stages use 0.5 micron recessed-gate NE 13783 FET's. The second stage is biased for low noise using the same input match. Output circuits of all FET stages are matched to 50 ohms using open-circuited parallel stubs to eliminate critical line spacing between stages. The remaining stages are biased at 50 percent I_{dss} and incorporate all 50 ohm lines with open-circuited parallel stubs at their inputs to achieve flat gain. The source leads of all FET's are soldered directly to ground pins located as close as possible under the FET's to eliminate inductive feedback effects.

Figure 6 illustrates the X-band amplifier gain and noise figure over a 10 percent frequency range. The overall noise figure of 2 dB includes the input waveguide isolator loss with coax transition (0.1 dB) coax hermetic feedthrough loss (0.1 dB), noise diode coupling loss (0.05 dB), limiter loss (0.4 dB), noise match loss (0.15 dB), and second-stage contribution (0.1 dB). The gain over the 10 percent bandwidth is flat to ± 0.2 dB at the 40 dB nominal gain value.

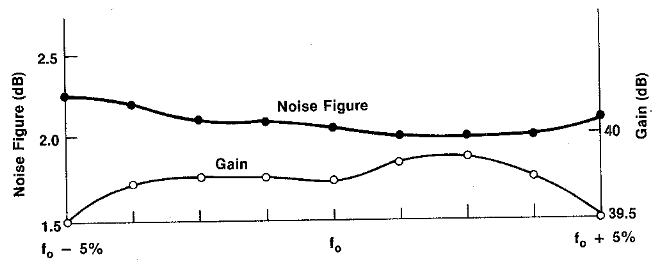


Figure 6. Noise Figure and Gain of X-Band Amplifier Including Two-Stage Limiter

CONCLUSIONS

Super-low-noise FET's combined with low-loss matching and new limiting circuits using soft substrate technology have led to a high performance, reproducible, and reliable low-noise amplifier.

REFERENCES

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2. J.J. Whalen and R.T. Kemerley, "X-Band Burnout Characteristics of GaAs MESFET's," *1982 IEEE MTT-S International Microwave Symposium Digest,* pp. 286-288.